ADCCONT PAGE 1

1 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

2 ;

3 ; Author : ADI - Apps www.analog.com/MicroConverter

4 ;

5 ; Date : October 2003

6 ;

7 ; File : ADCcont.asm

8 ;

9 ; Hardware : ADuC842/ADuC843

10 ;

11 ; Description : Performs ADC conversions in continuous mode at a

12 ; rate of 104KSPS.

13 ; Outputs ADC results into a buffer in ram.Continuously

14 ; flashes LED.

15 ; All rate calculations assume an 2.097152MHz Mclk.

16 ;

17 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

18

19 $MOD842 ; Use 8052&ADuC842 predefined symbols

20

00B4 21 LED EQU P3.4 ; P3.4 drives red LED on eval board

0000 22 CHAN EQU 0 ; convert this ADC input channel..

23 ; ..chan values can be 0 thru 8

24

25

---- 26 DSEG

0030 27 ORG 0030H

0028 28 LENGTH EQU 40

0030 29 BUFFER: DS LENGTH ; set up buffer in RAM

30

31 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

32 ; BEGINNING OF CODE

---- 33 CSEG

34

0000 35 ORG 0000h

36

0000 02004B 37 JMP MAIN ; jump to main program

38 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

39 ; INTERRUPT VECTOR SPACE

0033 40 ORG 0033H ; (ADC ISR)

0033 B85803 41 CJNE R0,#58H,CONT

0036 02003F 42 JMP EXIT ; place breakpoint here in debugger to view ram

after conversions

0039 A6DA 43 CONT: MOV @R0,ADCDATAH

003B 08 44 INC R0

003C A6D9 45 MOV @R0,ADCDATAL

003E 08 46 INC R0

003F 32 47 EXIT: RETI

48

49 ;====================================================================

50 ; MAIN PROGRAM

004B 51 ORG 004Bh

52

004B 53 MAIN:

54 ; PRECONFIGURE...

004B 75EFAC 55 MOV ADCCON1,#0ACh ; power up ADC /8 clk cycle + 16 cycles for conversion + 4 a

cq cycle

004E 75D800 56 MOV ADCCON2,#CHAN ; select channel to convert

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57

58 ; LAUNCH CONTINUOUS CONVERSIONS...

0051 7830 59 MOV R0,#BUFFER

0053 D2AF 60 SETB EA ; enable interrupts

0055 D2AE 61 SETB EADC ; enable ADC interrupt

0057 D2DD 62 SETB CCONV ; begin continuous conversions

63

64 ; CONTINUE WITH OTHER CODE...

0059 740A 65 MOV A,#10 ; delay length

005B B2B4 66 AGAIN: CPL LED ; blink (complement) the LED

005D 120062 67 CALL DELAY ; delay

0060 80F9 68 JMP AGAIN ; repeat

69

70 ; the micro is free to continue with other tasks (flashing the LED in

71 ; this case) while the ADC is continuously converting, and results

72 ; are being handled by the ADC interrupt service routine.

73

74 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

75 ; SUBROUTINE

0062 76 DELAY: ; Delays by 10ms \* A

77 ; 10mSec based on 2.09MHz

78 ; Core Clock

79 ;

80

0062 F9 81 MOV R1,A ; Acc holds delay variable (1 clock)

0063 7A1B 82 DLY0: MOV R2,#01Bh ; Set up delay loop0 (2 clocks)

0065 7BFF 83 DLY1: MOV R3,#0FFh ; Set up delay loop1 (2 clocks)

0067 DBFE 84 DJNZ R3,$ ; Dec R3 & Jump here until R3 is 0 (3 clocks)

0069 DAFA 85 DJNZ R2,DLY1 ; Dec R2 & Jump DLY1 until R2 is 0 (3 clocks)

006B D9F6 86 DJNZ R1,DLY0 ; Dec R1 & Jump DLY0 until R1 is 0 (3 clocks)

006D 22 87 RET ; Return from subroutine

88

89 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

90

91

92 END

VERSION 1.2h ASSEMBLY COMPLETE, 0 ERRORS FOUND

ADCCONT PAGE 3

ADCCON1. . . . . . . . . . . . . D ADDR 00EFH PREDEFINED

ADCCON2. . . . . . . . . . . . . D ADDR 00D8H PREDEFINED

ADCDATAH . . . . . . . . . . . . D ADDR 00DAH PREDEFINED

ADCDATAL . . . . . . . . . . . . D ADDR 00D9H PREDEFINED

AGAIN. . . . . . . . . . . . . . C ADDR 005BH

BUFFER . . . . . . . . . . . . . D ADDR 0030H

CCONV. . . . . . . . . . . . . . B ADDR 00DDH PREDEFINED

CHAN . . . . . . . . . . . . . . NUMB 0000H

CONT . . . . . . . . . . . . . . C ADDR 0039H

DELAY. . . . . . . . . . . . . . C ADDR 0062H

DLY0 . . . . . . . . . . . . . . C ADDR 0063H

DLY1 . . . . . . . . . . . . . . C ADDR 0065H

EA . . . . . . . . . . . . . . . B ADDR 00AFH PREDEFINED

EADC . . . . . . . . . . . . . . B ADDR 00AEH PREDEFINED

EXIT . . . . . . . . . . . . . . C ADDR 003FH

LED. . . . . . . . . . . . . . . NUMB 00B4H

LENGTH . . . . . . . . . . . . . NUMB 0028H

MAIN . . . . . . . . . . . . . . C ADDR 004BH

P3 . . . . . . . . . . . . . . . D ADDR 00B0H PREDEFINED